

RESUME

VIKAS KUMAR

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Objective

Highly motivated and detail-oriented B. Tech ECE graduate seeking an entry-level position as an RTL Design Engineer. Possess strong foundational knowledge in digital logic design, conventional and sequential circuits, FPGA, and FSM design. Proficient in Verilog, Testbench, and tools like Xilinx and HDL Bit. Skilled in C language, with excellent communication and problem-solving abilities.

Skills

- **Digital Logic Design:** Expertise in designing conventional and sequential circuits, flip-flops, adders, subtractors, mux/demux.
- **RTL Design:** Good understanding of FSM design and FPGA design flows.
- **Hardware Description Languages:** Proficient in Verilog and Testbench development.
- **Tools:** Hands-on experience with Xilinx, HDL Bit tools.
- **Computer Architecture:** Strong knowledge of computer architecture and digital system design principles.
- **Programming:**
 - **C Language:** Expertise in pointers, functions, and data structures.
 - **MS Excel:** Advanced proficiency in Excel for data analysis and reporting.
- **Soft Skills:** Excellent communication and teamwork skills, strong analytical thinking.

Education

Bachelor of Technology in Electronics and Communication Engineering

MIET, Meerut | 2021

Jammu Public Higher Secondary School, Jammu

Senior Secondary School | 2017

Projects

1. FSM-Based Traffic Light Controller (Verilog Project)

- Designed and simulated a finite state machine (FSM) for controlling a traffic light system.
- Implemented the project in Verilog and verified it using Testbench on Xilinx tools.
- Gained insights into state transitions and sequential circuit design.

2. 4-Bit Ripple Carry Adder/Subtractor (Verilog Project)

- Designed a 4-bit adder/subtractor using Verilog and simulated the design on Xilinx.
- Developed the Testbench to verify the functionality of both addition and subtraction.
- Strengthened understanding of digital arithmetic circuits and HDL design flows.

Certifications

- **Python for Everybody** – Coursera
- **SQL Fundamentals** – Udemy
- **CCNA** – Cisco
- **C Language** – MIET College

Languages

- English
- Hindi

Personal Details

- **Date of Birth:** 26/10/1998
- **Marital Status:** Single
- **Native Place:** Jammu

Declaration

I hereby declare that the above information is true and correct to the best of my knowledge and belief.

Signature: Vikas Kumar